

Fig. 1

FIG. 2 is a schematic diagram of a device 100, which includes a first electrode 10, a second electrode 20, and a dielectric layer 12 disposed between the first electrode 10 and the second electrode 20. The first electrode 10 is connected to a first terminal 26, and the second electrode 20 is connected to a second terminal 24. The dielectric layer 12 is disposed between the first electrode 10 and the second electrode 20. The first electrode 10 is connected to a first terminal 26, and the second electrode 20 is connected to a second terminal 24. The dielectric layer 12 is disposed between the first electrode 10 and the second electrode 20.

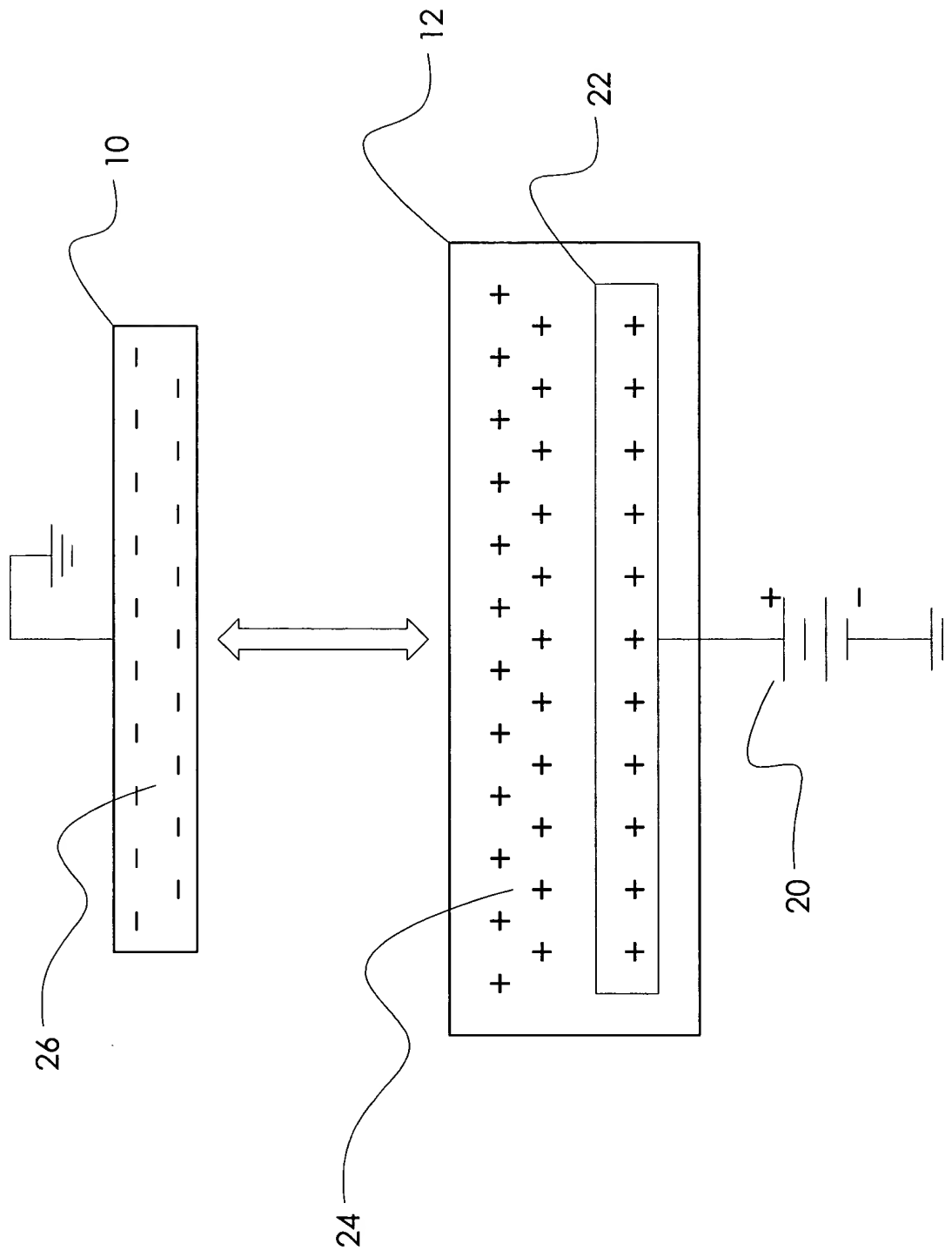


Fig. 2

FIG. 3 is a schematic diagram of a device 10, showing a top view of the device 10. The device 10 includes a substrate 12, a first conductive layer 30a, a second conductive layer 30b, a first insulating layer 32a, a second insulating layer 32b, a first gate electrode 34a, a second gate electrode 34b, a first gate insulating layer 36a, and a second gate insulating layer 36b. The first gate electrode 34a is connected to a first gate voltage source 30a, and the second gate electrode 34b is connected to a second gate voltage source 30b. The first gate insulating layer 36a is formed over the first gate electrode 34a, and the second gate insulating layer 36b is formed over the second gate electrode 34b. The first insulating layer 32a is formed over the first gate insulating layer 36a, and the second insulating layer 32b is formed over the second gate insulating layer 36b. The first conductive layer 30a is formed over the second insulating layer 32b, and the second conductive layer 30b is formed over the first insulating layer 32a.

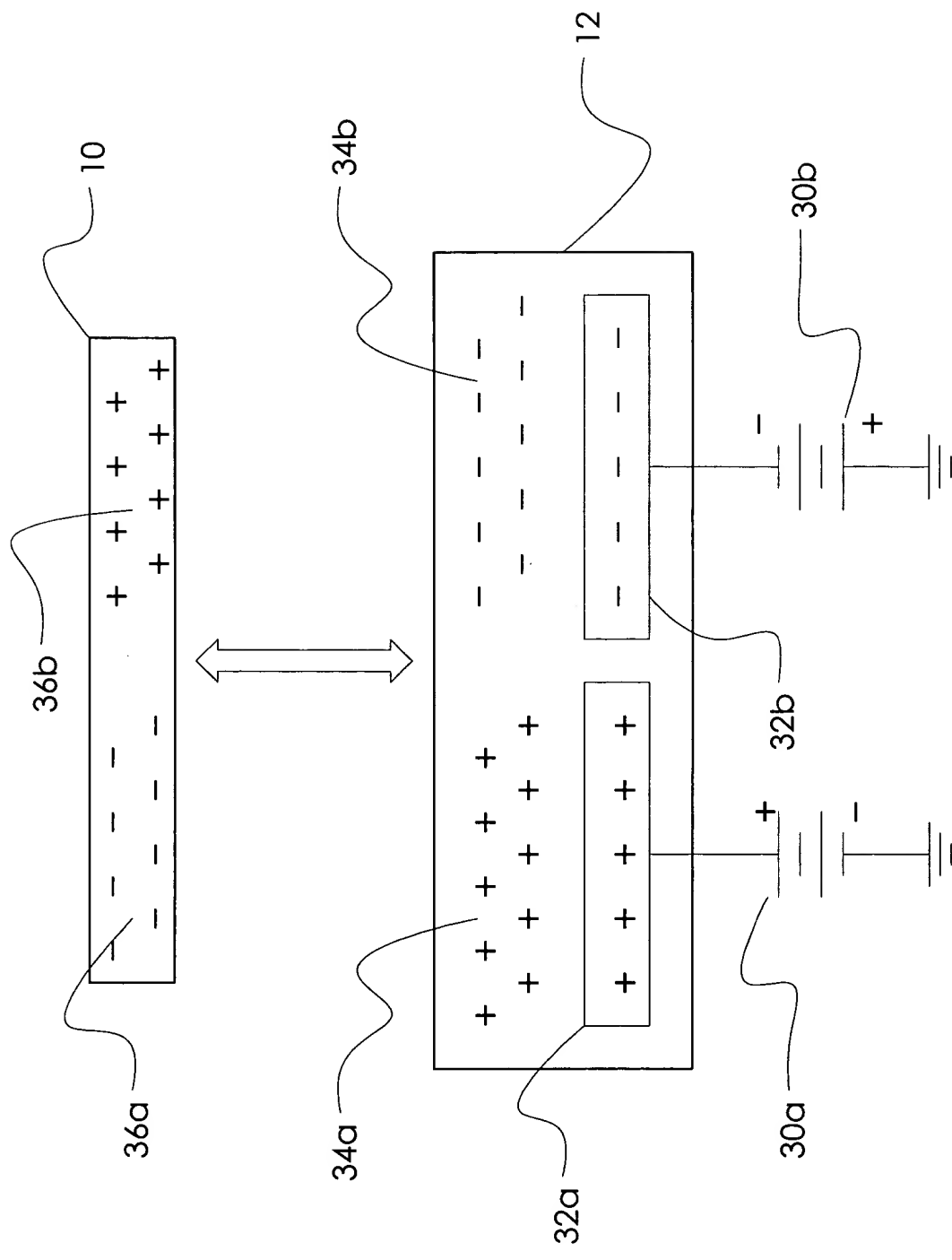


Fig. 3

FIG. 4 is a block diagram of a control system for a dual-channel system. The system includes a control system 46, two channels 40a and 40b, and a central processing unit 12. The control system 46 is connected to the channels 40a and 40b via lines 48. The channels 40a and 40b are connected to the central processing unit 12 via lines 42a and 42b. The central processing unit 12 is connected to a data bus 10 via lines 18a and 18b. The data bus 10 is connected to a power supply 80 via lines 82. The power supply 80 is connected to the channels 40a and 40b via lines 44.

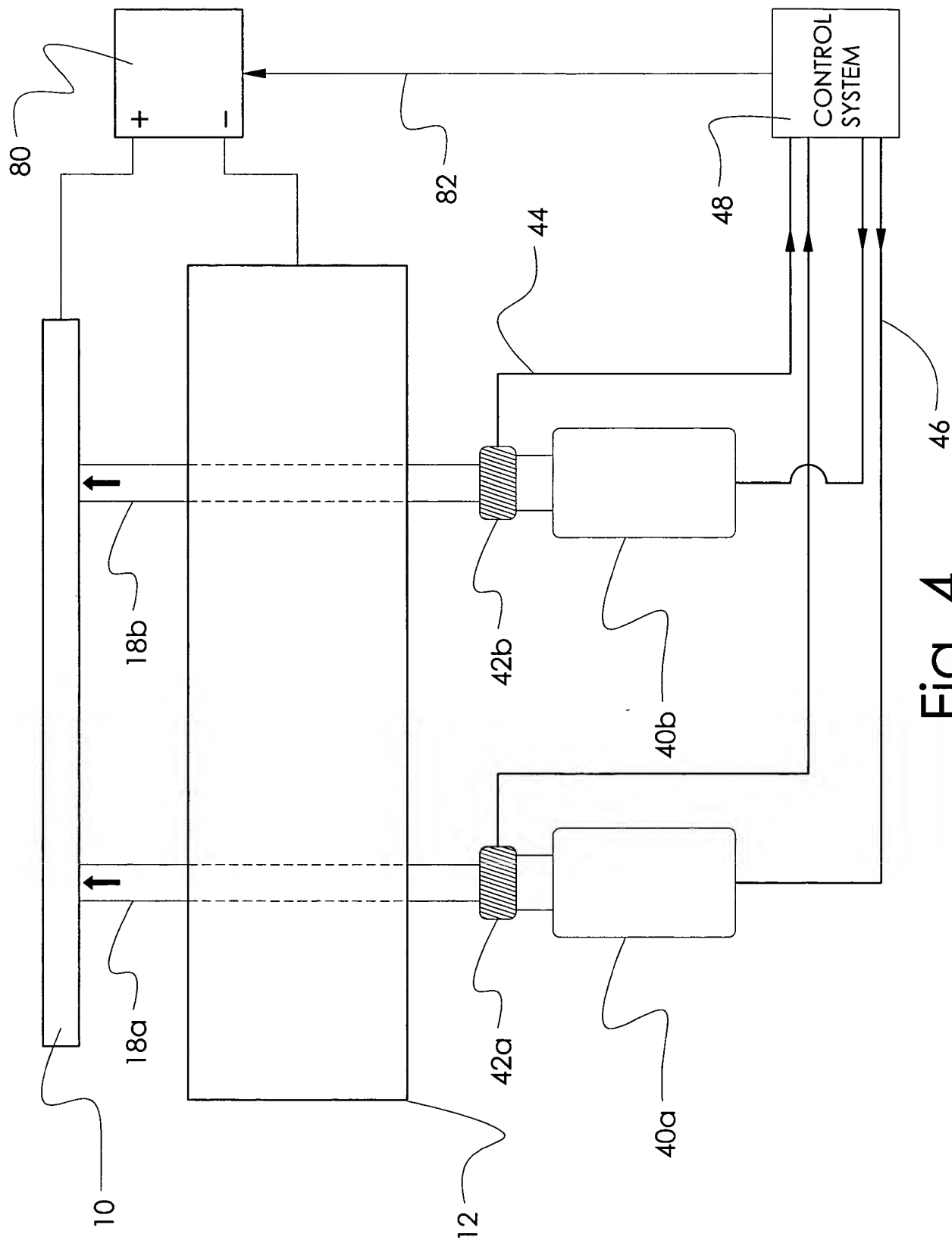


Fig. 4



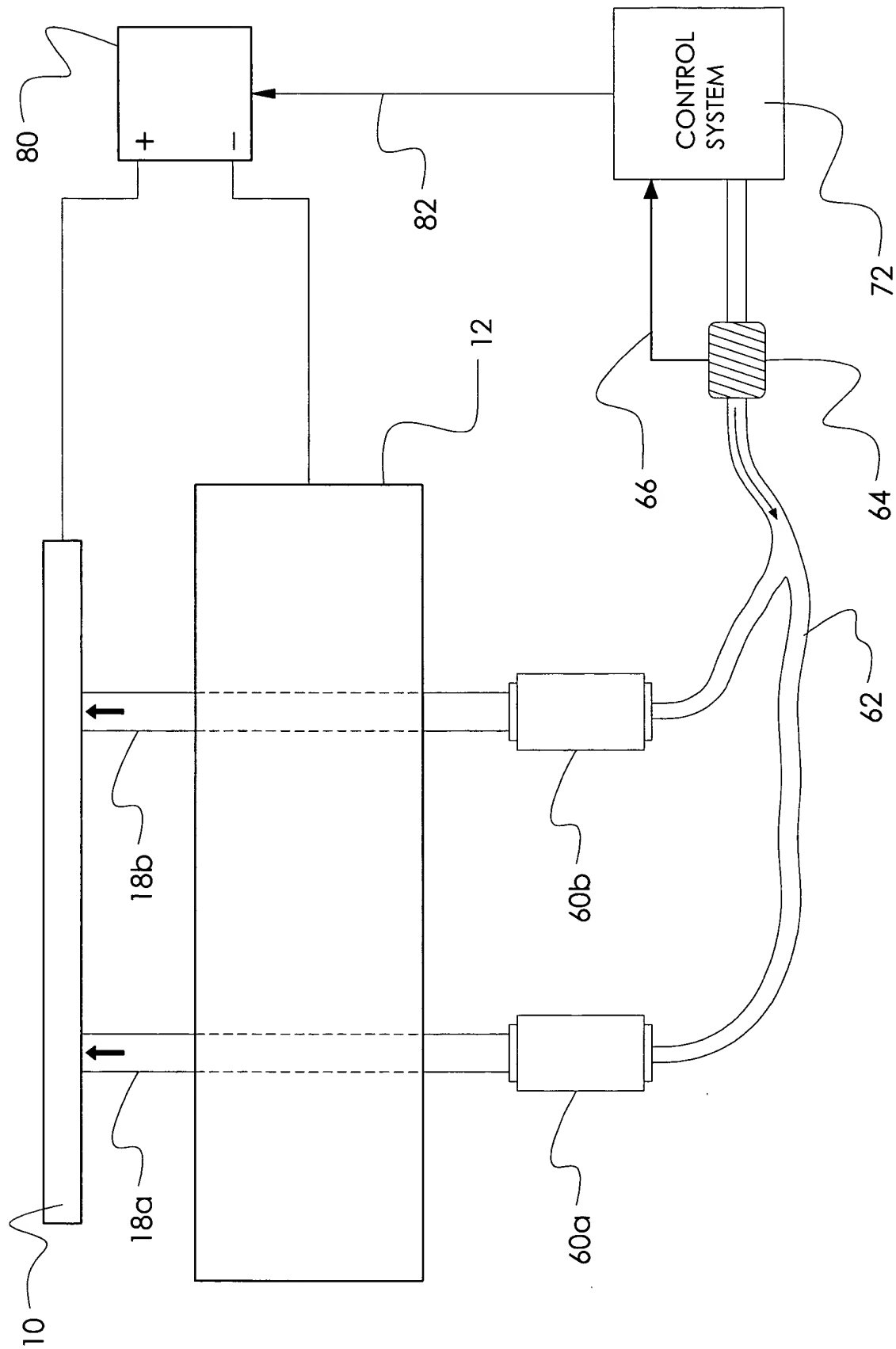


Fig. 6

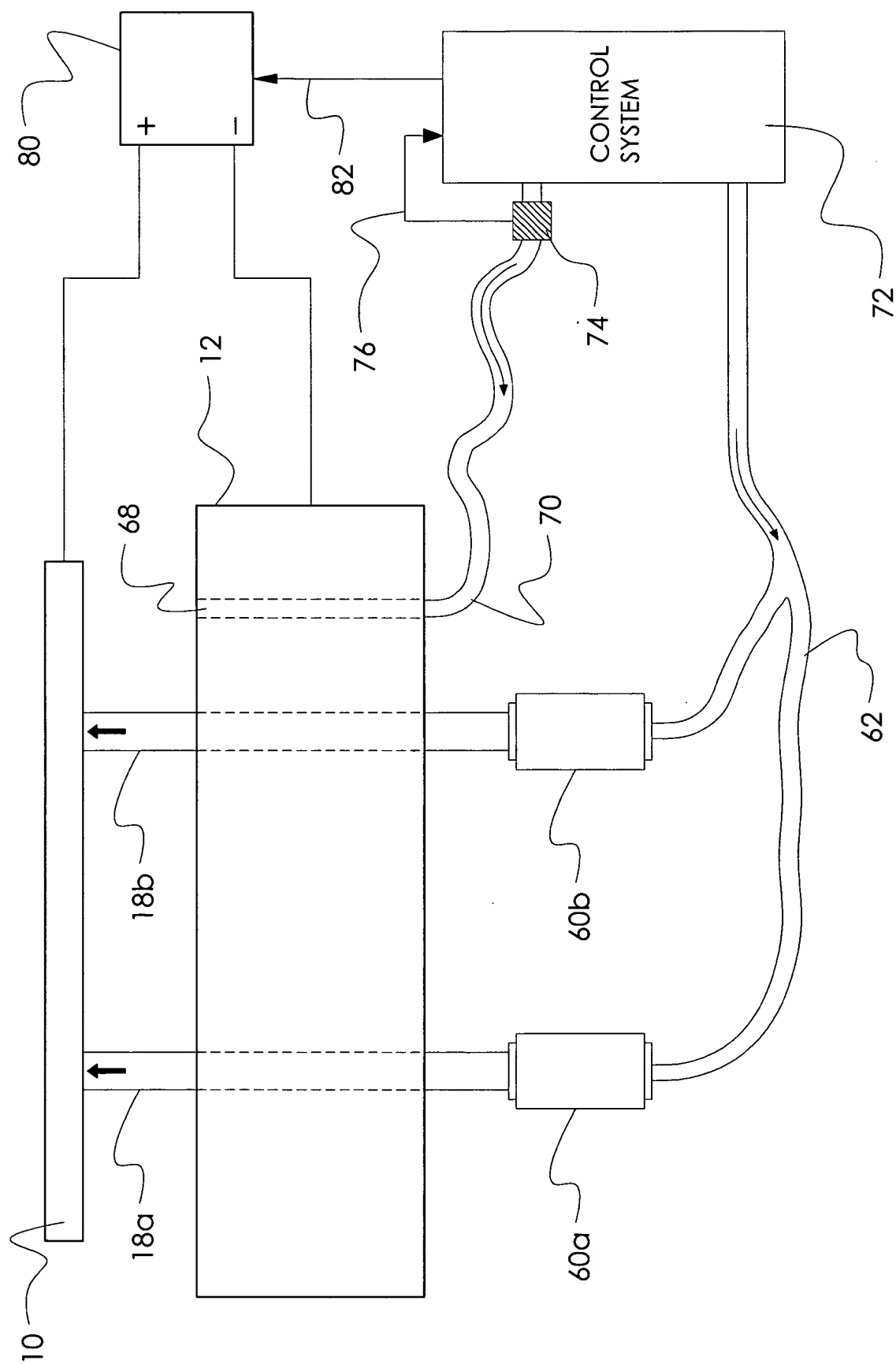


Fig. 7